

Low capacitance bidirectional TVS Diodes for ESD Protection

General Description

The PAExxxD3BA Series are low capacitance bidirectional TVS Diodes designed for applications requiring transient overvoltage protection capability. They are intended for use in voltage and ESD sensitive equipment such as computers, printers, business machines, communication systems, medical equipment and other applications. These devices are ideal for situations where board space is at a premium.

This series has been specifically designed to protect sensitive components which are connected to power, data and transmission lines from overvoltage caused by ESD(electrostatic discharge), and EFT (electrical fast transients).

Feature

- ◆ Peak Power Dissipation 350 W (8 x 20 us Waveform)
- Replacement for MLV (0805)
- Protects One Power or I/O Port
- Low Clamping Voltage
- Low Leakage
- lacktriangle Response Time is < 1 ns
- Available in Multiple Voltages Ranging From 3V to 36V
- Meets MSL 1 Requirements
- Solid-state silicon avalanche technology
- ROHS compliant

Application

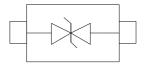
- Cellular handsets AND accessories
- Portable instrumentation
- Peripherals
- Networking and Telecom
- Serial and Parallel Ports
- Notebooks, Desktops, Servers
- Projection TV

Protection solution to meet

- IEC61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
- IEC61000-4-4 (EFT) 40A (5/50ns)

> <u>SOD-323</u>





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Maximum Ratings (TA=25°C Unless otherwise specified)

Parame	ter	Symbol	Value	Unit
Peak Pulse Power (tp=8/20μs wavefor	Рррр	350	Watts	
ESD Rating per IEC61000-4-2: Contact		±30		KV
	Air		±30	ΚV
Lead Soldering Temperature	$T_{\rm L}$	260 (10 sec.)	$^{\circ}$	
Operating Temperature Range	Tı	-55 ~ 150	$^{\circ}\mathbb{C}$	
Storage Temperature Range	Тѕтс	-55 ~ 150	$^{\circ}\mathbb{C}$	
Lead Solder Temperature – Maximun	$T_{\rm L}$	260	$^{\circ}\mathbb{C}$	

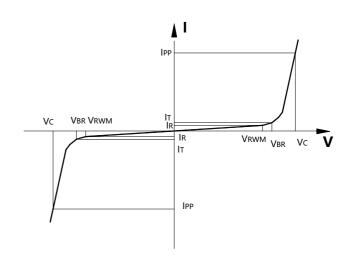
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

> Electrical Characteristics (TA=25°C Unless otherwise specified)

		X 7	I AV	V _{BR} @ 1 mA	v_{C1}	V_{C2}	I _{PP}	P _{PPP}	CJ
Device	Marking	V_{RWM}	I _R @ V _{RWM}	(Volts)	@ 1 A IPP	@IPP	(Amps)	(Watt)	(pF)
		(V)	(uA)	Min	(V)	(V)	Max.	Max.	(typ)
PAE3V3D3BA	2A	3.3	20	4.00	7.8	28	17	350	100
PAE5V0D3BA	2B	5	5	6	8	16	20	320	75
PAE5V0D3BA1	2B	5	5	6	8	10	20	250	75
PAE8V0D3BA	2F	8	1	8	9	12	18	200	54
PAE12VD3BA	AD	12	1	13.3	19	38	8	250	30
PAE15VD3BA	AE	15	1	16.7	24	45	5	250	22
PAE18VD3BA	2K	18	1	20.0	29	68	5	250	20
PAE24VD3BA	AF	24	1	26.1	43	79	3	250	12
PAE36VD3BA	AG	36	1	40.0	55	60	2.5	150	15

Junction capacitance is measured in VR=0V,F=1MHz

Symbol	Parameter			
Vrwm	Working Peak Reverse Voltage			
V _{BR}	Breakdown Voltage @ IT			
V _C	Clamping Voltage @ IPP			
I_{T}	Test Current			
IRM	Leakage current at VRWM			
Ірр	Peak pulse current			
Co	Off-state Capacitance			
CJ	Junction Capacitance			

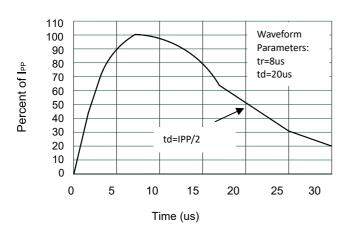


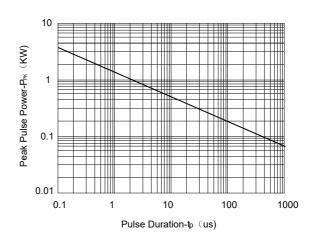
^{*}Other voltages may be available upon request.

^{1.} Non-repetitive current pulse, per Figure 1.

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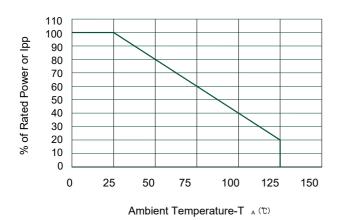
Typical Characteristics





Pulse Waveform

Non-Repetitive Peak Pulse Power vs. Pulse Time



Power Derating Curve

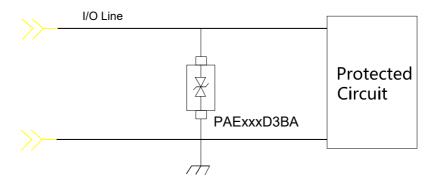
Ordering Information

Part Number	Description	Quantity		
PAE3V3D3BA~PAE36VD3BA	SOD-323 Reel	3000 pcs		

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Typical applications

I/O Line Protection



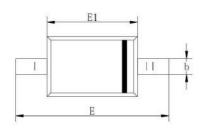
Circuit board layout and protection device placement

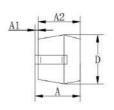
Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

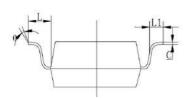
- 1. Place the protection device as close to the input terminal or connector as possible.
- 2. The path length between the protection device and the protected line should be minimized.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductor.
- 5. Minimize all printed-circuit board conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Ground planes should be used whenever possible. For multilayer printed-circuit boards, use ground vias.

Package Information (SOD-323)

CaseMaterial:MoldedPlastic.ULFlammabilit

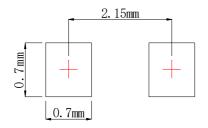




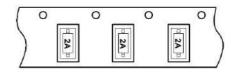


DIM	Millimeters				
DIM	Min	Max			
A	1.10Max				
A1	0.00	0.10			
A2	0.80	0.90			
b	0.25	0.35			
c	0.08	0.15			
D	1.20	1.40			
E1	1.60	1.80			
E	2.50	2.70			
L	0.475REF				
L1	0.25 0.40				

Recommended Pad outline



Device Orientation in Tape

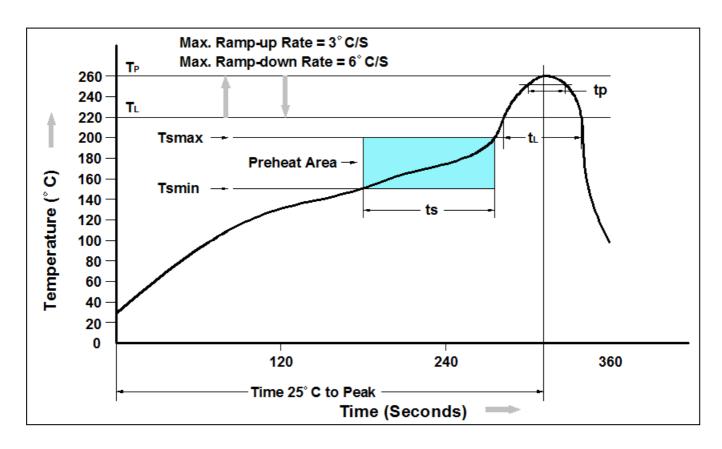


SOD-323 Reel Dim

Progressive direction Po Po Ko Planta Ao T

PACKAGE	W	E	F	P0	D	P2	P1	T	A0	В0	K0
SOD-323	8mm	1.75mm	3.5mm	4mm	1.5mm	2mm	4mm	0.23mm	1.5mm	3.0mm	1.25mm
SOD-323	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.05	±0.1	±0.1	±0.1

Recommand IR Reflow Soldering Thermal Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (ts) from (Tsmin to Tsmax)	60-120 seconds
Average Ramp-up Rate (tLto tP)	3°C/second max.
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60 – 150 seconds
Peak Temperature	260°C +0°C / -5°C
Time (tP) within 5°C of actual Peak Temperature	30 seconds
Ramp-down Rate (TP to TL)	6°C/second max
Time 25°C to Peak Temperature	8 minutes max.



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